

II. AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior listing of claims.

1. (Withdrawn) A method for generating a silicide resistor in one of a plurality of back-end-of-line (BEOL) layers without using high temperature processing, the method comprising the steps of:

forming a trough in an inter-layer dielectric (ILD) layer of the plurality of BEOL layers;
depositing a polysilicon layer over the trough;
etching the polysilicon layer to have a top surface below a surface of the ILD layer within the trough to form a polysilicon base in the trough;
depositing a first metal;
annealing to form a silicide layer from the first metal; and
planarizing to form a silicide section within the trough to generate the silicide resistor.

2. (Withdrawn) The method of claim 1, wherein the trough forming step includes patterning the ILD layer and etching to form the trough.

3. (Withdrawn) The method of claim 1, wherein the ILD layer includes one of: silicon dioxide (SiO₂), SiLK, boron doped oxide, and a high-k dielectric.

4. (Withdrawn) The method of claim 1, further comprising the step of forming one of a via through the ILD layer, and a wire in the ILD layer.

5. (Withdrawn) The method of claim 1, wherein an anneal temperature is lower than a damaging temperature that would damage a structure in the plurality of BEOL layers.
6. (Withdrawn) The method of claim 1, wherein the first metal is one of: cobalt (Co), palladium (Pd), platinum (Pt), nickel (Ni), molybdenum (Mo) and tungsten (W).
7. (Withdrawn) The method of claim 1, further comprising the step of forming a contact to the silicide section.
8. (Withdrawn) The method of claim 1, wherein the silicide section includes palladium silicide (PdSi) and has a resistivity of no less than approximately 25μ -ohms/cm and no greater than approximately 30μ -ohms/cm.
9. (Withdrawn) The method of claim 1, wherein the silicide section includes platinum silicide (PtSi) and has a resistivity of no less than approximately 26μ -ohms/cm and no greater than approximately 35μ -ohms/cm.
10. (Withdrawn) The method of claim 1, wherein the silicide section includes nickel silicide (NiSi) and has a resistivity of no less than approximately 14μ -ohms/cm and no greater than approximately 20μ -ohms/cm.

11. (Withdrawn) The method of claim 1, wherein the silicide section include di-nickel silicide (Ni_2Si) and has a resistivity of no less than approximately 35μ -ohms/cm and no greater than approximately 50μ -ohms/cm.
12. (Currently Amended) A resistor for a semiconductor device, the resistor comprising:
a silicide section positioned in a trough in one of a plurality of back-end-of-line (BEOL) layers;
wherein the silicide section has a silicidation temperature less than a damaging temperature of the plurality of BEOL layers.
13. (Original) The resistor of claim 12, wherein the silicide section includes cobalt silicide (CoSi) and has a resistivity of no less than approximately 14μ -ohms/cm and no greater than approximately 20μ -ohms/cm.
14. (Original) The resistor of claim 12, wherein the silicide section includes palladium silicide (PdSi) and has a resistivity of no less than approximately 25μ -ohms/cm and no greater than approximately 30μ -ohms/cm.
15. (Original) The resistor of claim 12, wherein the silicide section includes platinum silicide (PtSi) and has a resistivity of no less than approximately 26μ -ohms/cm and no greater than approximately 35μ -ohms/cm.

16. (Original) The resistor of claim 12, wherein the silicide section includes nickel silicide (NiSi) and has a resistivity of no less than approximately 14μ -ohms/cm and no greater than approximately 20μ -ohms/cm.

17. (Original) The resistor of claim 12, wherein the silicide section includes di-nickel silicide (Ni_2Si) and has a resistivity of no less than approximately 35μ -ohms/cm and no greater than approximately 50μ -ohms/cm.

18. (Original) The resistor of claim 12, wherein the silicide section includes one of molybdenum silicide (MoSi_2) and tungsten silicide (WSi_2).

19. (Original) The resistor of claim 12, further comprising a polysilicon base positioned below the silicide section.

20. (Currently Amended) A semiconductor device comprising:

a silicide resistor in one of a plurality of back-end-of-line (BEOL) layers, the silicide resistor including a silicide section having a silicidation temperature less than a damaging temperature of the plurality of BEOL layers;

wherein the silicide section is positioned in a trough in one of the plurality of back-end-of-line (BEOL) layers.